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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,384	09/11/2003	Geum-Jong Bae	239/169 DIV	3795

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/659,384	BAE ET AL.
	Examiner	Art Unit
	Hoai v. Pham	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/274,035.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 31 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation "wherein the surface insulating layer partially, but not completely, fills the undercut region and the L-shaped lower spacer completely fills the remainder of the undercut region" is not described in the specification and shown in the figure (see fig. 8 for details). See claim 26 that recites the second element extending from the first element laterally away from the T-shaped gate electrode. According to fig. 7, the second element extending from the first element laterally away from the T-shaped gate electrode does not fill the undercut region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 20-23 and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. [U.S. Pat. 6,500,743] newly cited, in view of Matsuda [U.S. Pat. 6,316,297] previously applied.

With respect to claims 20, Lopatin et al. discloses (fig. 24, cols. 2-9) a semiconductor device comprising:

a T-shaped gate electrode (104, 2402, 1604) disposed on a semiconductor substrate (102), the T-shaped gate electrode (104, 2402, 1604) having a wide portion (2402, 1604) and a narrow portion (104), the narrow portion disposed between the wide portion and the semiconductor substrate (102), so as to have an undercut region adjacent to the narrow portion;

an L-shaped lower spacer (124) covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode (104, 2402, 1604) and covering

sides of the wide portion of the T-shaped gate electrode (2402, 1604), the L-shaped lower spacer (124) having a first element disposed substantially perpendicular to the semiconductor substrate (102), and having a second element disposed substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode (104, 2402, 1604), wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer (124);

a low-concentration impurity region (130, 132) formed in the semiconductor substrate at both sides of T-shaped gate electrode (104, 2402, 1604); and

a high-concentration impurity region (110, 112) formed in the semiconductor substrate next to the L-shaped lower spacer (124).

Lopatin et al. fails to disclose a mid-concentration impurity region disposed between the high-and low-concentration impurity regions. However, Matsuda discloses that a mid-concentration impurity region (28) is disposed between the low-concentration impurity region (26) and high-concentration impurity region (34) (see fig. 3 and col. 9, lines 39-41). Therefore, it would have been obvious to one having ordinary skill in the art to modify the device of Lopatin et al. by having a mid-concentration impurity region disposed between the high- and low-concentration impurity regions as taught by Matsuda in order to provide the known purpose of lower electrical field thereby improving hot carrier performance.

With respect to claim 21, Lopatin et al. discloses that the T-shaped gate electrode (104, 2402, 1604) comprises lower (104) and upper conductive layer patterns (2402, 1604) are sequentially stacked, wherein the upper conductive layer pattern (2402, 1604) is wider than the lower conductive layer pattern (104) (see fig. 24).

With respect to claim 22, Lopatin et al. discloses that the L-shaped lower spacer (124) further comprises a third element (126) extending into the undercut region, the third element disposed substantially parallel to the semiconductor substrate and extending from the first element laterally towards the T-shaped gate electrode (see fig. 24).

With respect to claim 23, Lopatin et al. discloses that the lower and upper conductive layer patterns (104 and 2402, 1604) are made of materials having an etch selectivity with respect to each other (see col. 2, lines 20-25 and col. 9, lines 26-32).

With respect to claim 25, Lopatin et al. discloses that the upper conductive layer pattern (2402 same as layer 1602) is made of tungsten (see col. 8, lines 5-9).

With respect to claims 26, Lopatin et al. discloses (fig. 24, cols. 2-9) a semiconductor device comprising:

a T-shaped gate electrode (104, 2402, 1604) disposed on a semiconductor substrate (102), the T-shaped gate electrode (104, 2402, 1604) having a wide portion (2402, 1604) and a narrow portion (104), the narrow portion disposed between the wide

portion and the semiconductor substrate (102), so as to have an undercut region adjacent to the narrow portion;

an L-shaped lower spacer (124) covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode (104, 2402, 1604) and covering sides of the wide portion of the T-shaped gate electrode (2402, 1604), the L-shaped lower spacer (124) having a first element disposed substantially perpendicular to the semiconductor substrate (102), and having a second element disposed substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode (104, 2402, 1604), wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer (124);

a low-concentration impurity region (130, 132) formed in the semiconductor substrate at both sides of T-shaped gate electrode (104, 2402, 1604);

a high-concentration impurity region (110, 112) formed in the semiconductor substrate next to the L-shaped lower spacer (124); and

a surface insulating layer (126) intervened between the narrow portion of the gate electrode (104) and the L-shaped lower spacer (124).

Lopatin et al. fails to disclose a mid-concentration impurity region disposed between the high-and low-concentration impurity regions. However, Matsuda discloses that a mid-concentration impurity region (28) is disposed between the low-concentration impurity region (26) and high-concentration impurity region (34) (see fig. 3 and col. 9, lines 39-41). Therefore, it would have been obvious to one having ordinary skill in the

art to modify the device of Lopatin et al. by having a mid-concentration impurity region disposed between the high- and low-concentration impurity regions as taught by Matsuda in order to provide the known purpose of lower electrical field thereby improving hot carrier performance.

With respect to claim 27, Lopatin et al. discloses that the first element of the L-shaped lower spacer (124) completely covers sides of the wide portion (2402, 1604) of the T-shaped gate electrode (104, 2402, 1604) (see fig. 24).

With respect to claim 28, Lopatin et al. discloses that the second element of the L-shaped lower spacer (124) partially covers the narrow portion (104) of the T-shaped gate electrode (104, 2402, 1604) (see fig. 24).

With respect to claim 29, Lopatin et al. discloses that thicknesses of the first and second elements are approximately the same (see fig. 24).

With respect to claim 30, Lopatin et al. discloses that the surface insulating layer (126) completely fills the undercut region (see fig. 24).

With respect to claim 31, as best understood, Lopatin et al. discloses that wherein the surface insulating layer (126) completely fills the undercut region and the L-shaped lower spacer (124) completely covers the undercut region (see fig. 24).

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. [U.S. Pat. 6,500,743] newly cited, in view of Matsuda [U.S. Pat. 6,316,297] previously applied as applied to claim 20 above, and further in view of Furukawa et al. [U.S. Pat. 6,891,235] previously applied.

Lopatin et al. in view of Matsuda substantially disclose all the limitations as claimed above except the lower conductive layer pattern (104) is made of silicon gemanium or nitride titanium. However, Furukawa et al. discloses that these materials, silicon gemanium or nitride titanium, and their uses are well-known in the art for forming the lower conductive layer pattern (56) (see fig. 6 and col. 5, lines 65-67). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to select silicon gemanium as known materials, as taught by Furukawa et al., into the device of Lopatin et al. to form the lower conductive layer pattern. Moreover, selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945).

7. Claims 20-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 6,891,235] previously applied, in view of Matsuda [U.S. Pat. 6,316,297] previously applied and Lopatin et al. [U.S. Pat. 6,500,743] newly cited.

With respect to claims 20, Furukawa et al. discloses (fig. 3e, cols. 4-5) a semiconductor device comprising:

a T-shaped gate electrode (20) disposed on a semiconductor substrate (21), the T-shaped gate electrode (20) having a wide portion (26) and a narrow portion (22), the narrow portion disposed between the wide portion and the semiconductor substrate (21), so as to have an undercut region adjacent to the narrow portion;

an L-shaped lower spacer (48) covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode (20) and covering sides of the wide portion of the T-shaped gate electrode (20), the L-shaped lower spacer (48) having a first element disposed substantially perpendicular to the semiconductor substrate (21), and having a second element disposed substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode (20);

a low-concentration impurity region (34) formed in the semiconductor substrate at both sides of T-shaped gate electrode (20); and

a high-concentration impurity region (50) formed in the semiconductor substrate next to the L-shaped lower spacer (48).

Furukawa et al. fails to disclose a mid-concentration impurity region disposed between the high-and low-concentration impurity regions (50 and 34). However, Matsuda discloses that a mid-concentration impurity region (28) is disposed between the low-concentration impurity region (26) and high-concentration impurity region (34) (see fig. 3 and col. 9, lines 39-41). Therefore, it would have been obvious to one having ordinary skill in the art to modify the device of Furukawa et al. by having a mid-concentration impurity region disposed between the high- and low-concentration

impurity regions as taught by Matsuda in order to provide the known purpose of lower electrical field thereby improving hot carrier performance.

Furukawa et al. fails to disclose wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer. However, Lopatin et al. discloses that it is conventional for the L-shaped lower spacer (124) with the first element and the second element intersect to define a substantially 90 degree angle in an outer surface (see fig. 24). Moreover, it would have been an obvious matter of design choice to form the L-shaped lower spacer with the 90 degree angle in an outer surface as applicant claimed, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1995). Therefore, it would have been obvious to one having ordinary skill in the art to modify the L-shaped lower spacer of Lopatin et al. with the 90 degree angle in an outer surface.

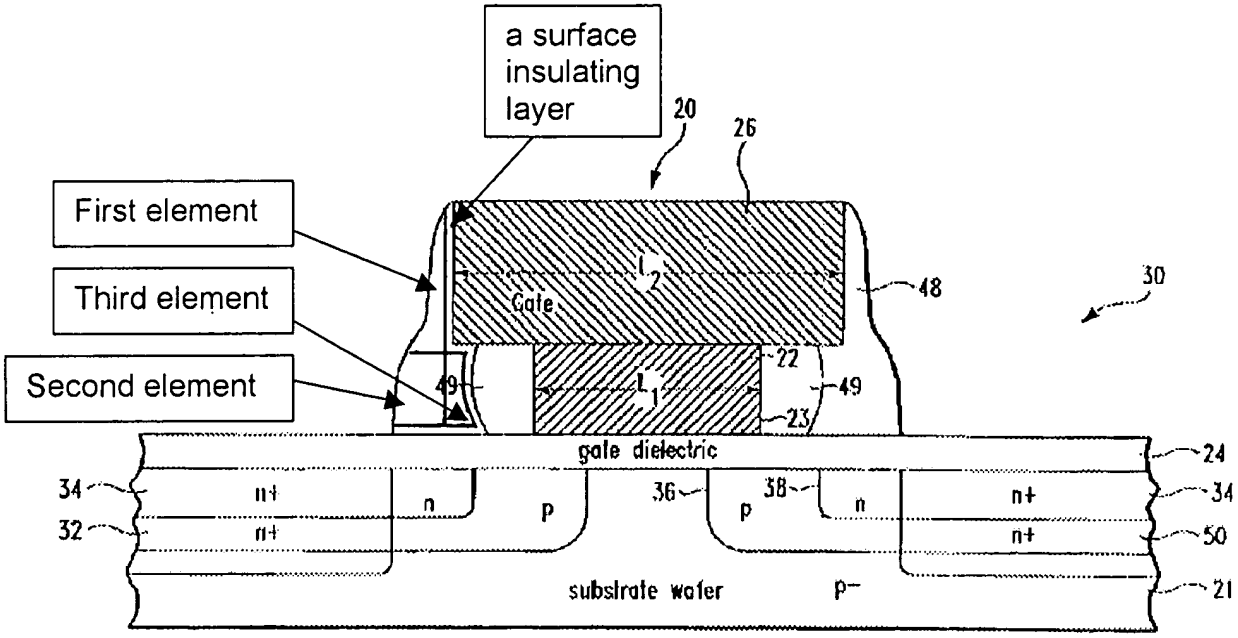

FIG. 3e

With respect to claim 21, Furukawa et al. discloses that lower and upper conductive layer patterns (22 and 26) are sequentially stacked, wherein the upper conductive layer pattern (26) is wider than the lower conductive layer pattern (22) (see fig. 3e).

With respect to claim 22, Furukawa et al. discloses that the L-shaped lower spacer (48) further comprises a third element extending into the undercut region, the third element disposed substantially parallel to the semiconductor substrate and extending from the first element laterally towards the T-shaped gate electrode (fig. 3e).

With respect to claim 23, Furukawa et al. discloses that the lower and upper conductive layer patterns (56 and 58) are made of materials having an etch selectivity with respect to each other (see col. 5, lines 31-36).

With respect to claim 24, Furukawa et al. discloses that lower conductive layer pattern (56) is made of silicon germanium (see col. 5, lines 65-67).

With respect to claim 25, Furukawa et al. discloses that the upper conductive layer pattern (58) is made of polysilicon (see col. 5, lines 34-35).

With respect to claim 26, Furukawa et al. discloses that a surface insulating layer (48) intervened between the gate electrode (20) and the lower spacer (48) (see fig. 3e). **Notice: as interpreting the claim in a broad scope, a surface insulating layer can also be the same as the lower spacer because the claims do not distinct the material of the lower spacer and the surface insulating layer. Therefore, the lower spacer and the surface insulating layer are considered as one layer.

With respect to claim 27, Furukawa et al. discloses that the first element of the L-shaped lower spacer (48) completely covers sides of the wide portion (26) of the T-shaped gate electrode (20) (see fig. 3e).

With respect to claim 28, Furukawa et al. discloses that the second element of the L-shaped lower spacer (48) partially covers the narrow portion (22) of the T-shaped gate electrode (20) (see fig. 3e).

With respect to claim 29, Furukawa et al. in view of Matsuda substantially disclose all the limitations as claimed above except thicknesses of the first and second elements are approximately the same. However, the thickness range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, it appears that these changes produce no functional differences and therefore would have been obvious. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

8. Applicant's arguments with respect to claims 20-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER